What is claimed is:

1. An active matrix display device having a display region consisting of sub-pixels arrayed in a matrix fashion, the sub-pixels having switching elements, comprising:

a plurality of data and scan signal lines, and common voltage lines for sending signals and a reference voltage to the sub-pixels;

first test transistors, each of which is connected to one of the plurality of scan signal lines for sending first test signals thereto; and

a plurality of first input terminals, each of which is connected to one of a plurality of the first test transistors;

wherein each gate of the first test transistors and each of the common voltage lines are connected to one of the first input terminals, the first test transistors control inputs of the first test signals to the sub-pixels.

2. The device as claimed in claim 1, wherein each of the sub-pixels comprises:

a switching transistor having a gate coupled to one of the scan signal lines, a drain/source coupled to one of the data signal lines; and

a storage capacitor coupled between one of the common voltage lines and a source/drain of the switching transistor.

3. The device as claimed in claim 1 further comprising:

a data driver generating the data signals; and

a scan driver generating the scan signals.

4. The device as claimed in claim 1 further comprising:

second test transistors, each of which is connected to one of the plurality of the data signal lines for sending second test signals thereto; and

a plurality of second input terminals, each of the second input terminals is connected to one of a plurality of the second test transistors;

wherein each gate of the second test transistors and each of the common voltage lines are connected to one of the second input terminals, the second test transistors control inputs of the second test signals to the sub-pixels.

5. A liquid crystal display panel comprising:

an array substrate on which an active matrix display device is formed, wherein the active matrix display device comprises:

a plurality of data and scan signal lines, and common voltage lines for sending signals and a reference voltage to the sub-pixels;

test transistors, each of which is connected to one of the plurality of scan signal lines for sending test signals thereto; and

a plurality of input terminals, each of which is connected to one of a plurality of the test transistors;

wherein each gate of the test transistors and each of the common voltage lines are connected to one of the input terminals, the test transistors control inputs of the test signals to the sub-pixels;

a facing substrate having a common electrode; and

a liquid crystal sealed between the array and facing substrate.

6. The panel as claimed in claim 5, wherein each of the sub-pixels further comprises:

a switching transistor having a gate coupled to one of the scan signal lines, a drain/source coupled to one of the data signal lines; and

a storage capacitor coupled between one of the common voltage lines and a source/drain of the switching transistor.

7. The panel as claimed in claim 5, wherein the active matrix display device further comprises:

a data driver generating the data signals; and

a scan driver generating the scan signals.

8. An active matrix display device having a display region consisting of sub-pixels arrayed in a matrix fashion, the sub-pixels having switching elements, comprising:

a plurality of data and scan signal lines, and common voltage lines for sending signals and a reference voltage to the sub-pixels;

test transistors, each of which is connected to one of the plurality of scan signal lines for sending test signals thereto; and

a plurality of input terminals, each of which is connected to one of a plurality of the test transistors;

wherein each gate of the test transistors and each of the common voltage lines are connected to one of the input terminals, the test transistors control inputs of the test signals to the sub-pixels, the display region is composed of a plurality of blocks, the scan signal lines included in a first block of the plurality of blocks are connected to a first set of the input terminals via sources/drains of the test transistors, and the scan signal lines included in a second block of the plurality of blocks are connected to a second set of the input terminals different from the first set of the input terminals via the sources/drains of the test transistors.

9. An active matrix display device comprising:

an array substrate having sub pixel sections arrayed in a matrix fashion, each sub pixel section having a switching element, the array substrate including:

a plurality of data signal lines and a plurality of scan signal lines for sending signals to the sub pixel sections;

test transistors, each of which is connected to one of the plurality of scan signal lines for sending test signals thereto; and

a plurality of input terminals for inputting the test signals;

wherein drains or sources of the test transistors are connected to the scan signal lines, gates of a plurality of the test transistors and the common voltage lines are connected to a first input terminal of the plurality of input terminals, the sources or drains of a plurality of the test transistors are connected to a second input terminal of the plurality of input terminals, and the test transistors control inputting of the test signals to the sub pixel sections.

10. The active matrix display device as claimed in claim 9, wherein the switching elements of the sub pixel sections and the test transistors are thin film transistors formed of amorphous silicon.

11. The active matrix display device as claimed in claim 9, wherein the sources or drains of the test transistors that are connected to adjacent ones of the data signal lines are connected to different ones of the plurality of input terminals.

12. The active matrix display device as claimed in claim 9, wherein the sources or drains of the test transistors that are connected to adjacent ones of the scan signal lines are connected to different ones of the plurality of input terminals.

13. The active matrix display device as claimed in claim 9, wherein the gates of all of the test transistors connected to the scan signal lines on the array substrate are connected to the first input terminal.

14. The active matrix display device as claimed in claim 9, further comprising: a drive circuit connected to the plurality of data signal lines and the plurality of scan signal lines, wherein when the drive circuit controls inputting of a screen display signal, all of the test transistors are held in an OFF state.

15. The active matrix display device as claimed in claim 9, further comprising an opposing substrate opposite to the array substrate.

16. An active matrix display device having a display region consisting of sub-pixels arrayed in a matrix fashion, the sub-pixels having switching elements, comprising:

a plurality of data and scan signal lines, and common voltage lines for sending signals and a reference voltage to the sub-pixels;

first test transistors, each of which is connected to one of the plurality of scan signal lines for sending first test signals thereto;

second test transistors, each of which is connected to one of the plurality of data signal lines for sending second test signals thereto; and

a plurality of first and second input terminals, each of the first input terminals is connected to one of a plurality of the first test transistors and each of the second input terminals is connected to one of a plurality of the second test transistors;

wherein each gate of the first test transistors and each of the common voltage lines are connected to one of the first input terminals, each gate of the second test transistors and each of the common voltage lines are connected to one of the second input terminals, the first and second test transistors control inputs of the first and second test signals to the sub-pixels.

17. An active matrix display device having a display region consisting of sub-pixels arrayed in a matrix fashion, the sub-pixels having switching elements, comprising:

a plurality of data and scan signal lines, and common voltage lines for sending signals and a reference voltage to the sub-pixels;

test transistors, each of which is connected to one of the plurality of data signal lines for sending test signals thereto; and

a plurality of input terminals, each of which is connected to one of a plurality of the test transistors;

wherein each gate of the test transistors and each of the common voltage lines are connected to one of the input terminals, the test transistors control inputs of the test signals to the sub-pixels.

18. A method for driving an active matrix display device having a display region consisting of sub-pixels arrayed in a matrix fashion, the sub-pixels having switching elements, the method comprising the steps of:

sending signals and a reference voltage to the sub-pixels through a plurality of data and scan signal lines, and common voltage lines;

sending first test signals to one of the plurality of scan signal lines through test transistors; and

sending second test signals to gates of the test transistors;

wherein the second test signals are used as the reference voltage sent to the pixel through the common voltage lines when the test transistors are turned off by the second test signals.

19. A display circuit comprising:

a pixel array having pixels each of said pixels coupled to a first, a second and a third line to receive a scan signal, a data signal and a common voltage respectively; and

a plurality of transistors having drains/sources coupled to the first lines, sources/drains coupled to receive first signals and gates commonly coupled to receive a second signal;

wherein the transistors are turned on by the second signal so that the first signals are transmitted on the first lines to drive the pixels during a test, and the transistors are turned off by the second signal so that the first signals are isolated from the first lines and the second signal is used as the common voltage supplied to the pixels through the third lines beyond the test.

20. The circuit as claimed in claim 19, wherein each of the pixels comprises:

a second transistor having a gate coupled to one of the first lines, a drain/source coupled to the second line; and

a storage capacitor coupled between one of the third lines and a source/drain of the second transistor.

21. The circuit as claimed in claim 19 further comprising:

a data driver generating the data signals; and

a scan driver generating the scan signals.

22. A liquid crystal display panel comprising:

an array substrate on an LCD circuit is formed, wherein the LCD circuit comprises:

a pixel array having pixels each of said pixels coupled to a first, a second and a third line to receive a scan signal, a data signal

and a common voltage respectively, and each of the pixels has a pixel electrode; and

a plurality of transistors having drains/sources coupled to the first lines, sources/drains coupled to receive a first signal and gates coupled to receive a second signal;

wherein the transistors are turned on by the second signal so that the first signals are transmitted on the first lines to drive the pixels during a test, and the transistors are turned off by the second signal so that the first signals are isolated from the first lines and the second signal is used as the common voltage supplied to the pixels through the third lines beyond the test;

a facing substrate having a common electrode; and

a liquid crystal sealed between the array and facing substrate.

23. The panel as claimed in claim 22, wherein each of the pixels further comprises:

a second transistor having a gate coupled to one of the first lines, a drain/source coupled to the second line; and

a storage capacitor coupled between one of the third lines and a source/drain of the second transistor.

24. The panel as claimed in claim 22, wherein the LCD circuit further comprises:

a data driver generating the data signals; and

a scan driver generating the scan signals.